REMARKS

Reconsideration and allowance of this application are respectfully requested in light of the above amendments and the following remarks.

Claims 1-3 and 8-10 have been amended to clarify the claimed invention and to place the claims in closer compliance with U.S. format.

Regarding the objections in the Office Action, Fig. 5 is hereby amended to label it as "prior art." Fig. 6 has not been labeled prior art because the Applicants note that not all of the subject matter of Fig. 6 is in the prior art.

Regarding the objection to the drawings under Rule 83(a) for not showing every feature of the invention specified in the claims, the Applicants respectfully submit that the original drawings do show the exposed faces of the outer lead portion arranged in a same level as an outer face of said sealing resin. The Applicant notes the description in the specification at page 18, lines 1-10, in conjunction with Fig. 3. The level refers to the side edge of resin 15 and the outer lead portion 16 being substantially flush with this side edge, as explained in the referenced portions of the specification and illustrated in Fig. 3.

Claims 1 and 8 were rejected as being indefinite for failing to particularly point out and distinctly claim Applicant's inventions, with reference to the process of upsetting.

In response, the Applicants note that the terminology of "upsetting process" means that a die pad portion is formed in a position higher than the inner lead. The Applicants submit that the process is not indefinite and is adequately disclosed in both the specification at page 17, lines 10-21 and the drawings, item 9, portions 11 and 13. The Applicants note in Fig. 3 the step portion 17 of item 9 and further note that the existence of step 17 allows for resin 15 to exist below die pad portion 11.

Accordingly, reconsideration and withdrawal of the rejection under 35 USC 112, second paragraph, is respectfully requested.

Turning now to the prior art rejections, claims 1, 7 and 8 stand rejected under 35 USC 102(d) as anticipated by Morihiro (JP '946). Claims 2-6 and 9-15 stand rejected under 35 USC 103(a) as unpatentable over Morihiro in view of Kanji (JP '952). It is noted that although the 102 rejection cites subsection "d," this should apparently be subsection "b" since the publication date is October 1990. Also, while the Office Action cites JP '925 to Kanji (no such reference is of record), this is construed as referring to JP '952 to Kanji which is of record. Insofar as these references may be applied against amended claims 1-3 and 8-

10 and original claims 4-6, and the claims dependent therefrom, the Applicants respectfully traverse.

The inventions described in claims 1 and 2 as amended includes a feature that "the die pad portion is smaller in size than the semiconductor chip." This specific feature in construction of the resin molded semiconductor provides the advantages of enabling sealing resin to be present on the bottom surface of the chip as well and thus a better balance of interactive forces between the chip surfaces and sealing resin will be achieved and, as a result, a decrease in mechanical damages of the semiconductor chip due to deformation such as bending.

The invention of claim 3 as amended includes a feature that a connecting portion of the metal wire to the inner lead portion is disposed between the groove portions and the contact surface of the inner lead portion to the thin metal wire is flat. This specific feature in construction of the resin molded semiconductor device provides advantage in that the stress imposed to the connecting portion of the fine metallic wire located between grooves is distributed evenly to each of the adjacent grooves and thus the stress imposed to the thin metal wire can further be alleviated.

The invention of claim 4 includes a feature that a widened portion is formed in each of the inner lead portions. This particular feature provides advantages in that the anchor effect of

the sealing resin to the device is enhanced, thus enhancing the stress imposed to either the lead portion of the product device or the thin metal wire by preventing separation of either lead wire or metal wire and enabling the reliability of the device to be maintained.

The invention of claim 5 includes a feature that a widened portion is formed in each of the inner lead portions and at least one groove portion is formed in a surface. This particular feature provides the advantage of further enhancing the anchor effect of the sealing resin to the device with alleviation of the stress imposed to either the lead portion of the product device or the thin metal wire by preventing separation of either lead wire or metal wire, thus enabling maintenance of device reliability.

The invention of claim 6 includes a feature that a widened portion is formed in each of the inner lead portions and that a connecting portion the metal wire to the inner lead portion is disposed between the groove portions. This specific feature in construction of the resin molded semiconductor device provides advantages in that the interactive force caused by taking a structure of sealing one side of the lead frame is absorbed by the groove portions avoiding a stress in the intermediate portions between adjacent grooves. Thus, a stable connection is achieved

eliminating destruction of the connection between the lead frame and fine metallic wire.

As noted above, claims 1, 7 and 8 stand rejected under 35 U.S.C. §102(b) as being anticipated by Morihiro and claims 2-6 and 9-15 stand rejected under §103(a) as being obvious over Morihiro in view of Kanji. The Applicants respectfully submit that all pending claims patentably distinguish over these references, considered alone or in combination, for at least the following reasons.

The semiconductor device disclosed in the Morihiro references comprises a semiconductor chip 1 mounted on a pad portion (island) 2 of a lead frame, bonding wires 3 which electrically connect the electrodes of the semiconductor chip 1 respectively to the inner side of a lead frame 4, and a resin body 8 which surrounds and seals the peripheral region of the semiconductor chip 1.

The peripheral region of the semiconductor chip 1 includes a wire connecting portion on the upper surface of the semiconductor chip 1 and the pad portion (island) 2. The outer side of the lead frame 4 is disposed on the bottom surface of the resin body 8 and the pad portion (island) 2 is located in a higher position than the inner side of the lead frame 4.

Kanji teaches that a bonding pad 4 of a semiconductor chip is electronically connected to the grooves 7 formed on the surface of the inner lead 1b.

Present claims 1, 2 and 8 recite that the die pad portion is smaller in size than the semiconductor chip. As described in the preceding section, this specific feature in construction of the resin molded semiconductor device provides advantages in that the sealing resin is able to be present on the bottom surface of the chip as well and thus better balance of interactive forces between the chip surfaces and sealing resin will be achieved. As a result mechanical damages of the semiconductor chip to deformation such as bending can be diminished.

There is neither description nor suggestion about this particular feature of the invention in the Morihiro reference. Morihiro does not refer to the dimensional relationship of the semiconductor chip 1 to the island 2. Figure 2(b) of Morihiro shows the semiconductor chip 1 smaller in size than island 2.

According to the structure of the semiconductor device disclosed by Morihiro, the sealing resin is not present on the bottom side of the chip allowing contact of the resin body 8 only to its surfaces. Consequently, the interactive force of the resin body 8 is imposed exclusively to the contacting surfaces of the chip 1, resulting in an unstable distribution of the interactive forces. Thus, Morihiro will not achieve the specific effect of present claims 1, 2 and 8, which is previously described above, of sealing resin present on the bottom surface of the chip as well,

with a better balance of interactive forces between the chip surface and sealing resin will be achieved and as a result a reduction in mechanical damages of the chip due to deformation such as bending. Such is not an effect exerted by the semiconductor device of Morihiro.

Claims 3, 9 and 10 have a common feature in construction of the molded semiconductor device of the invention, in that a connecting portion of the metal wire to the inner lead portion is disposed between or adjacent to the groove portions and the contact surface of the inner lead portion to the fine metallic wire is flat. This specific feature in construction of the resin molded semiconductor device provides advantages wherein the stress imposed to the grooves is distributed evenly to each of the adjacent grooves. Thus, the stress imposed to the thin metal wire can be further alleviated. Additionally, connectivity in the wire-bonding process is improved.

In Morihiro and Kanji, there is neither a description nor a suggestion of these characteristic features of claims 3, 9 and 10. Particularly, Kanji discloses a technology where the contact surface of the bonding wire 5 to the inner lead 1b is increased by contacting the bonding wire 5 to the surfaces of a plurality of grooves 7 of the inner lead. The technology is not intended for mitigation of the stress by the presence of two adjacent grooves

between which the connecting portion to the thin metal wire is located.

Further, in the disclosure of Kanji a plurality of grooves 7 are formed on the surface of the inner lead 1b to which the bonding wire 5 is connected. This disclosure does not imply that these grooves 7 are positioned so that the connecting portion is located between adjacent grooves. Thus, this structure does not provide the advantages of the present invention where the stress imposed to the connecting portion of the fine metallic wire located between grooves is distributed evenly to each of the adjacent grooves.

Further, in the particular configuration of the resin molded semiconductor device of claims 3, 9 and 10, the surface of the inner lead portion to which the thin metal wire is connected is flat so that bonding of the thin metal wire to the surface of the inner lead can be made in a stable manner. On the other hand, according to the disclosure of Kanji, a plurality of grooves 7 are formed on the bonding surface of the inner lead 1b, which surface is not flat.

Claims 4, 5 and 6 have a common feature in that a widened portion is formed in each of the inner lead portions. This particular feature further enhances the anchor effect of the sealing resin to the device and alleviates the stress imposed to either the lead portion of the product device or the thin metal

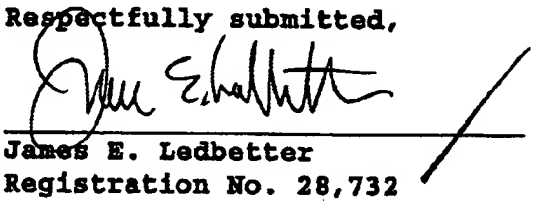
wire by preventing separation of either lead wire or thin metal wire, thus maintaining the reliability of the device.

In either of the references of Morihiro or Kanji, there is no description nor suggestion of this feature of claims 4, 5 and 6. Further, there is no disclosure of anything relating to increasing contact area between an inner lead portion and sealing resin for enhancing the anchor effect in the inner lead portion.

For at least the above reasons, it is respectfully submitted that all grounds of rejection stated in the Office Action have been overcome. A Notice of Allowance is respectfully solicited.

If any issues remain which may be best resolved through a telephone communication, the Examiner is requested to kindly telephone the undersigned at the local, Washington D.C. telephone number listed below.

Respectfully submitted,



James E. Ledbetter
Registration No. 28,732

Date: April 22, 2002

JEL/KJW/att

ATTORNEY DOCKET NO. JEL 30763 PCT

STEVENS, DAVIS, MILLER & MOSHER, L.L.P.
Suite 850
1615 L Street, N.W.
Washington, D.C. 20036
Telephone: (202) 408-5100
Facsimile: (202) 408-5200

Exhibit I - Marked Up Claims

Please amend claims 1-3 and 8-10 as follows:

1. (Amended) A resin molded type semiconductor device comprising: a semiconductor chip which is mounted on a die pad portion of a lead frame; thin metal wires which electrically connect terminals of an upper face of said semiconductor chip to inner lead portions of the lead frame; a sealing resin which seals an outer peripheral region of said semiconductor chip, said region including a thin metal wire region of the upper face of said semiconductor chip, and a lower region of said die pad portion; and outer lead portions which are arranged in a bottom face region of said sealing resin, [and characterized in that] wherein said lead frame is subjected to an upsetting process so that said die pad portion is located at a position higher than said inner lead portions and said die portion is smaller in size than said semiconductor chip.

2. (Amended) A resin molded type semiconductor device comprising: a semiconductor chip which is mounted on a die pad portion of a lead frame; thin metal wires which electrically connect terminals of an upper face of said semiconductor chip to inner lead portions of said lead frame; a sealing resin which seals an outer peripheral region of said semiconductor chip, said region

including a thin metal wire region of the upper face of said semiconductor chip; and outer lead portions which are arranged in a bottom face region of said sealing resin and which are formed to be continuous to respective inner lead portions, [and characterized in that] wherein at least one groove portion is formed in a surface of each of said inner lead portions and said die portion is smaller in size than said semiconductor chip.

3. (Amended) A resin molded type semiconductor device comprising: a semiconductor chip which is mounted on a die pad portion of a lead frame; thin metal wires which electrically connect terminals of an upper face of said semiconductor chip to inner lead portions of said lead frame; a sealing resin which seals an outer peripheral region of said semiconductor chip, said region including a thin metal wire region of the upper face of said semiconductor chip; and outer lead portions which are arranged in a bottom face region of said sealing resin and which are formed to be continuous to respective inner lead portions, [and characterized in that] wherein a plurality of groove portions are formed in a surface of each of said inner lead portions, [and] a connecting portion of said thin metal wire on a side of said inner lead portion is disposed between said groove portions and an area in a

surface of said inner lead portion at which said thin metal wire is contacted is flat.

8. (Amended) A method of manufacturing a resin molded type semiconductor device, said method comprising the steps of: performing an upsetting process on a lead frame so that a die pad portion is located at a position higher than inner lead portions; bonding a semiconductor chip which is larger in size than said die pad portion to said die pad portion of said lead frame; electrically connecting terminals of said semiconductor chip to said inner lead portions of said lead frame by thin metal wires; sealing an outer peripheral region of said semiconductor chip, thereby forming a sealing resin, said region including a region of an upper face of said semiconductor chip and electrically connected by said thin metal wires, and a lower region of said die pad portion; and shaping outer lead portions of the lead frame so as to be exposed from an outer face of said sealing resin.

9. (Amended) A method of manufacturing a resin molded type semiconductor device [characterized in that], said method [comprises] comprising the steps of: bonding a semiconductor chip to a lead frame having inner lead portions in each of which a widened portion is disposed and having a flat surface in which at

least one groove portion is formed [in a surface]; electrically connecting terminals of said semiconductor chip to said inner lead portions of said lead frame by thin metal wires; sealing an outer peripheral region of said semiconductor chip, thereby forming a sealing resin, said region including a region of an upper face of said semiconductor chip and electrically connected by said thin metal wires, and a lower region of said semiconductor chip; and shaping outer lead portions of said lead frame so as to be exposed from an outer face of said sealing resin, and, when said terminals of said semiconductor chip are to be electrically connected to said inner lead portions by said thin metal wires, the connection is performed while connecting portions of said thin metal wires on the side of said inner lead portions are disposed [in the vicinity of] at the flat surface adjacent said at least one groove portion.

10. (Amended) A method of manufacturing a resin molded type semiconductor device [characterized in that], said method [comprises] comprising the steps of: bonding a semiconductor chip to a lead frame having inner lead portions in each of which a widened portion is disposed and having a flat surface in which a plurality of groove portions are formed [in a surface]; electrically connecting terminals of said semiconductor chip to said inner lead portions of said lead frame by thin metal wires;

sealing an outer peripheral region of said semiconductor chip, thereby forming a sealing resin, said region including a region of an upper face of said semiconductor chip and electrically connected by said thin metal wires, and a lower region of said semiconductor chip; and shaping outer lead portions of said lead frame so as to be exposed from an outer face of said sealing resin, and, when said terminals of said semiconductor chip are to be electrically connected to said inner lead portions by said thin metal wires, the connection is performed while connecting portions of said thin metal wires on the side of said inner lead portions are disposed in the flat surface between said plurality of groove portions.